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1993 J. Phys.: Condens. Matter 5 L227

(http://iopscience.iop.org/0953-8984/5/16/002)

J. Phys.: Condens. Matter 5 (1993) L227–L234. Printed in the UK

LETTER TO THE EDITOR

Electron conduction characteristics of split-gate structures fabricated on pseudomorphic GaAs–$In_xGa_{1-x}As$–AlGaAs heterostructures

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Received 19 February 1993

Abstract. Sub-micron split-gate structures have been fabricated on three pseudomorphic GaAs–$In_xGa_{1-x}As$–AlGaAs quantum well structures, with indium fraction, x of 0.04, 0.10, and 0.14. The conductance characteristic of the device on the $x = 0.04$ material showed clear plateaux due to the quantization of ballistic conduction in one dimension. Devices fabricated from the $x = 0.10$ and $x = 0.14$ material did not show plateaux, but exhibited a complex structure that varied quantitatively between nominally identical devices. This structure is thought to be due to both the random nature of the $In_xGa_{1-x}As$ alloy, and the roughness of the $In_xGa_{1-x}As$ interfaces. The spatial variation of the potential between the arms of the split gate due to these effects was probed by applying a differential voltage between the two gates.

The high mobility of a two-dimensional electron gas (2DEG) formed at a GaAs–AlGaAs heterostructure allows effects due to the ballistic conduction of electrons to be observed in small structures. The 2DEG may be further confined to a one-dimensional (1D) wire by applying a negative bias to a metal split gate fabricated on the surface of the wafer (Thornton *et al* 1986). Provided the device length is very much shorter than the electron elastic scattering length, plateaux in the device resistance associated with 1D ballistic transport may be observed (Wharam *et al* 1988, van Wees *et al* 1988). The conductance, G, of such a device transmitting electrons through n one-dimensional channels is given by

$$G = 2ne^2/h. \tag{1}$$

InGaAs based systems are of interest because of their low effective mass, and their potential applications in the opto-electronics industry. In this letter, we report the observation of plateaux in the resistance of split-gate devices fabricated on GaAs–$In_xGa_{1-x}As$–AlGaAs strained quantum well wafers. An undoped GaAs buffer layer was grown by molecular beam epitaxy at 570 °C on semi-insulating GaAs substrate followed by 10 nm of undoped $In_xGa_{1-x}As$, the active layer. This was capped with 1 nm GaAs to prevent diffusion of indium whilst the temperature was ramped to 640 °C over 90 seconds for growth of the subsequent layers. A 20 nm undoped $Al_{0.33}Ga_{0.67}As$ spacer layer was grown before a 40 nm

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0953-8984/93/160227+08$07.50

silicon doped $Al_{0.33}Ga_{0.67}As$ layer. The 2D carrier density after brief illumination of each $In_xGa_{1-x}As$ quantum well was between 4×10^{15} m^{-2} and 7×10^{15} m^{-2}. The layers were capped by 10 nm of undoped GaAs. Six structures were grown; the indium fraction, x, was varied from 0 to 0.25 in steps of 0.05. High quality pseudomorphic layers were obtained for $x \leqslant 0.20$; that with $x = 0.25$ was relaxed, and dislocated. Further growth and characterization details are given in Mace *et al* (1993). The single-particle electron elastic scattering lengths, deduced from the amplitude of the Shubnikov–de Haas oscillations, were in excess of 0.2 μm for the wafers with $x \leqslant 0.20$ suggesting that it might be possible to observe 1D effects using split gates with lengths of this order. The mobilities, and electron scattering lengths, are shown in figure 1. The mobility of the samples with $x > 0$, in which alloy scattering is dominant, lie approximately on a line given by $C/(x(1-x))$, as predicted by alloy scattering models (Walukiewicz *et al* 1984).

Four sizes of split-gate devices with lengths of 0.1 μm and 0.3 μm and gate separations of 0.4 μm and 0.5 μm were fabricated on wafers with $x = 0.04$, $x = 0.10$, and $x = 0.15$, using standard electron-beam lithography. The conductance characteristics of the devices were measured using a constant AC voltage of 10 μV between source and drain. All devices on the same wafer were qualitatively similar; the difference between the devices is thought to be due to differences in the microstructure of the semiconductor layers beneath each split gate. Figure 2 shows the conductance characteristics of the 0.1 μm long split gate with 0.4 μm gate separation on the $x = 0.04$ wafer at a temperature of 100 mK. A series resistance has been subtracted from the data. This series resistance is slightly larger than that measured when the gates are defined. It is assumed that on definition an additional spreading resistance is induced in the vicinity of the gates.

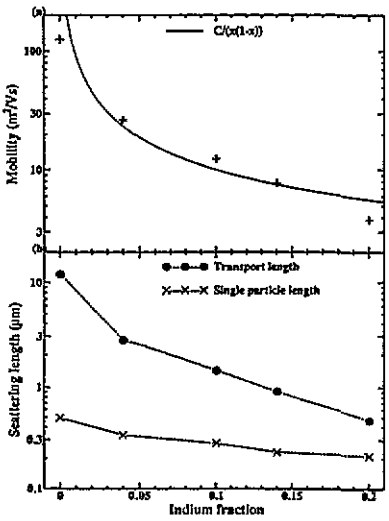

Figure 1. (i) The mobility of the wafers after brief illumination as a function of indium fraction, x. The solid line is a guide to the eye showing the $1/(x(1-x))$ dependence appropriate to alloy scattering. (ii) The electron scattering lengths as a function of indium fraction after illumination. The transport length is calculated from the zero-field resistivity and carrier density; the single particle length is derived from the amplitude of the Shubnikov–de Haas oscillations (Coleridge *et al* 1988).

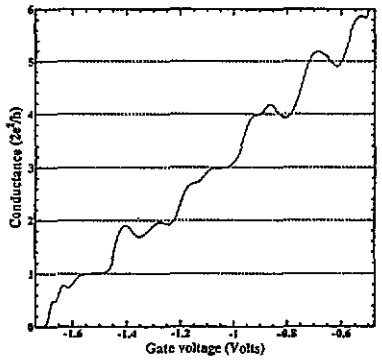

Figure 2. The conductance characteristic of a split gate on the $x = 0.04$ material at $T = 100$ mK.

Structure is observed in the conductance characteristic at values corresponding to one-dimensional ballistic plateaux. This structure was investigated further by sweeping the 1D channel between the arms of the split gate by applying a differential voltage between them (Stroh and Pepper 1989). These data are shown in figure 3. Each curve of the graph corresponds to sweeping the arms of the split gate simultaneously with a constant offset voltage between the arms. The bold central line is the conductance characteristic for zero-offset voltage, shown in figure 2. Each curve is offset from the centre by half the voltage difference between the arms. This offset voltage was incremented by 50 mV for each curve.

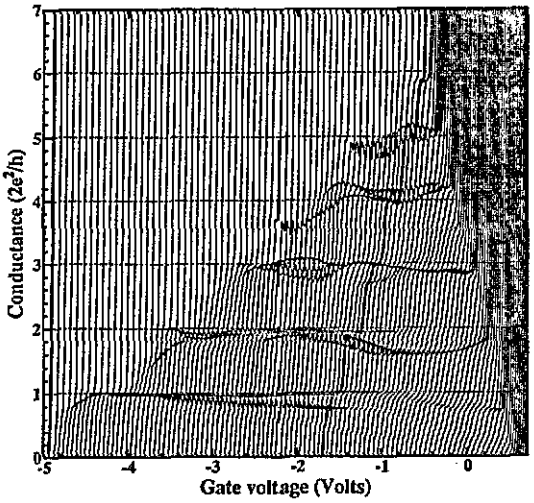

Figure 3. The conductance versus gate voltage of a split gate on the $x = 0.04$ material at $T = 100$ mK. The spacing in offset voltage between each line is 50 mV. The solid line is for zero offset (as shown in figure 2). Each line is displaced from the zero by half the offset voltage.

The plateaux due to one-dimensional ballistic conduction of electrons through the split gate can be clearly seen. However, it is also clear that some other mechanism is modifying the conductance characteristics, leading to a displacement of the plateaux from the values

given by equation (1) and also giving rise to additional resonance-like structure on the plateaux.

An estimate of the 1D subband spacing was made by measuring the conductance at fixed gate voltage as a function of DC bias across the device (Patel *et al* 1991). Glazman and Khaetskiĭ (1989) predict that if the DC bias is dropped symmetrically across the split gate, then additional plateaux spaced at e^2/h intervals are resolved when the bias voltage is approximately equal to the one-dimensional subband spacing. In this situation, the first subband above the Fermi energy conducts in one direction only.

Figure 4 shows the variation of the differential conductance with DC bias voltage at successive fixed gate voltages at a temperature of 100 mK. The voltage dropped across the 2DEG on either side of the device has been subtracted from the data. The curves at higher conductances are shortened because this voltage is more significant in this region. The convergence of the lines at $n = 1$ and $n = 2$ around zero DC bias are due to the 1D plateaux spaced at $2e^2/h$ intervals. The clustering at $n = 3/2$ and $n = 5/2$ observed at finite DC bias is evidence for additional quantization and gives a 1D subband spacing of order 2 meV for the values of gate voltage used in the measurement. This figure is of the same magnitude as that obtained by other workers (Wharam *et al* 1989, Patel *et al* 1991, van Wees *et al* 1991).

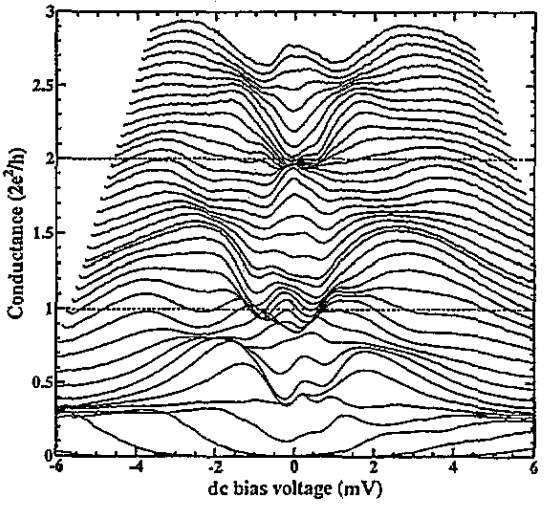

Figure 4. The conductance versus DC bias voltage of a split gate for various fixed split-gate voltages.

The conductance characteristics of the split gates on the $x = 0.10$, and $x = 0.14$ wafers were measured at zero DC bias, again sweeping the 1D channel between the arms of the split gate using the differential voltage method. These data are shown in figures 5 and 6. The $x = 0.10$ device is 0.3 μm long with 0.4 μm gate separation; that on the $x = 0.14$ wafer is 0.1 μm long with 0.4 μm gate separation. The data for $x = 0.10$ appears to show some structure associated with the $n = 1$ plateau, but plateaux corresponding to higher values of n are masked. For the $x = 0.14$ wafer, the 1D plateaux are completely masked by structure that is also a function of the 1D channel position. In all the devices measured, the structure was entirely reproducible, but was quantitatively different for different devices. The structure

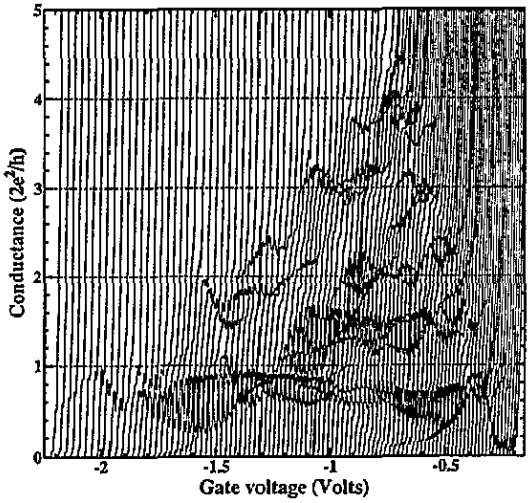

Figure 5. The conductance versus gate voltage of a split gate on the $x = 0.10$ material at $T =$ 100 mK. The spacing in offset voltage between each line is 20 mV.

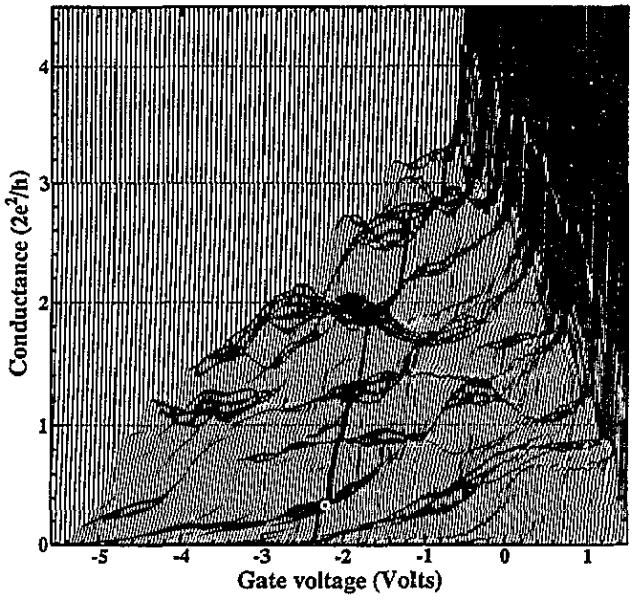

Figure 6. The conductance versus gate voltage of a split gate on the $x = 0.14$ material at $T =$ 300 mK. The spacing in offset voltage between each line is 10 mV.

was also changed following brief illumination with a red LED, and on thermally cycling the device.

A rough estimate of the spatial extent of the potential causing the additional structure may be made by examining the persistence of structure across the data shown in figures 3, 5 and 6. If the depletion width of the split-gate arms when first defined is equal to the gate–2DEG separation, then the region between the vertical gate definition lines in these figures

corresponds to sweeping the 1D channel across approximately 0.26 μm. For $x = 0.10$, structure persists approximately half way between these limits, corresponding to a spatial extent of about 100 nm. For $x = 0.14$, the spatial extent of the structure is 40–50 nm.

The temperature dependence of the structure on the $x = 0.10$ wafer was investigated, and is shown in figure 7. The base temperature of the dilution refrigerator was 17 mK. However, as a constant AC voltage of 10 μV was used, the electron temperature in the device did not fall below 100 mK. Figure 5 shows that the structure is visible at 500 mK. Complete blurring of the structure occurs between 750 mK and 1 K. The energy distribution width of the electrons may be estimated by $4k_BT$ (van Wees *et al* 1991) suggesting that the energy separation associated with the additional structure is of order 0.2–0.5 meV. This is approximately 5–10 times less than the 1D subband spacing in typical split-gate devices.

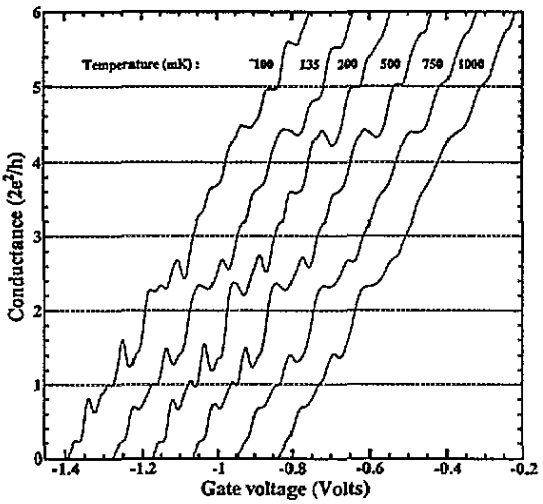

Figure 7. The temperature dependence of the conductance characteristics of a split gate on the $x = 0.10$ material. The minimum electron temperature is 100 mK.

Some structure, as opposed to perfectly flat plateaux, was observed in all the devices measured. Resonant structure at the falling edge of 1D plateaux are predicted by Szafer and Stone (1989). However, these resonances arise from the non-adiabatic constriction considered. Because of the separation between the gate and 2DEG, it is unlikely that the potential defining the 1D region will be abrupt. Moreover, it is usual to treat the potential landscape within split-gate structures fabricated on GaAs–AlGaAs as adiabatic and the introduction of indium to the active layer should not change this. Resonance structure in the conductance characteristics may also be introduced by the presence of scatterers. Chu and Sorbello (1989) and Bagwell (1990) show that an attractive impurity represented by a delta-function may give rise to resonances at the plateaux. Resonances may also arise if the saddle-shaped potential along the axis of the split gate is modified such that minima, containing localized states, occur within the split gate.

A number of physical mechanisms that might give rise to the structure may be ruled out. Although the $In_xGa_{1-x}As$ layers are not lattice-matched to the GaAs substrate, there is no evidence that there are a significant number of dislocations within the wafers that could cause the additional structure in the conductance characteristics. The $In_xGa_{1-x}As$ layers in these wafers are well below the critical thickness at which dislocations are predicted

to form (Matthews and Blakeslee 1974). Photoluminescence data and magneto-transport measurements suggest that the layers are strained and have low dislocation densities (Mace *et al* 1993). TEM analysis gives an upper limit for the dislocation density of 10^6 cm^{-2} which is far too small to cause the additional structure observed.

Significant incorporation of indium into the AlGaAs donor layer as a result of segregation and diffusion has not occurred. SIMS analysis (Mace *et al* 1993) showed no trace of indium within the AlGaAs, and only very slight indium contamination of the wafer surface (of order 0.1%). Thus the structure is not due to additional scattering by indium atoms acting as remote impurity scatterers.

It is proposed that the structure in the conductance characteristics is a result of modification of the split-gate potential due to both the random nature of the $In_xGa_{1-x}As$, and interface roughness effects. Because there is little ordering of the indium and gallium atoms within the alloy, clustering of the indium atoms may occur. This will produce local minima in the crystal potential, which will give rise to resonant structure in the conductance characteristics. The structure observed in the $x = 0.10$ and $x = 0.14$ devices appears similar to that calculated by Schwalm and Schwalm (1992) for a 1D channel with rough surfaces. There are several mechanisms that are likely to increase the interface roughness scattering at the $In_xGa_{1-x}As$ quantum well interfaces. Sakaki *et al* (1987) have shown that interface surface roughness scattering time is proportional to the sixth power of the quantum well width for GaAs/AlGaAs samples. Thus, interface roughness scattering is likely to be significant, although not dominant, in these samples. The diffusion length of indium at an MBE grown interface can be of order 3 nm (Muraki *et al* 1993), and such interfaces are rarely smooth, again reducing the interface roughness scattering time. Finally, the control GaAs–AlGaAs sample grown with a long growth interrupt at the hetero-interface showed an enhanced dependence of mobility on carrier density over similar samples grown without interrupt. This suggests that the growth interrupt causes slight degradation of the surface, and thus an increase in the interface roughness scattering (Foxon *et al* 1986).

In conclusion, split-gate devices have been fabricated on GaAs–$In_xGa_{1-x}As$–AlGaAs pseudomorphic quantum well wafers. Devices on the $x = 0.04$ wafer showed plateaux due to the ballistic conduction of electrons in one dimension. Devices on the higher indium concentration wafers showed additional random, but reproducible structure. This additional structure is thought to be due to the random nature of the arrangement of the indium and gallium atoms within the $In_xGa_{1-x}As$, and roughness of the GaAs–$In_xGa_{1-x}As$ and $In_xGa_{1-x}As$–AlGaAs interfaces caused by indium diffusion.

We would like to thank Dr E H Linfield for assistance in the running of the MBE machine. This work was supported by the Science and Engineering Research Council. DAR acknowledges the support of the Toshiba Cambridge Research Centre Ltd.

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